Design of Low Noise 10 GHz divide–by–16…511 Frequency Divider

M. Jurgo[1], K. Kiela[1], R. Navickas[1]

1Departament of Computer Engineering, Vilnius Gediminas Technical University,
Naugarduko st. 41-439, LT-03227 Vilnius, Lithuania
marijan.jurgo@vgtu.lt

Abstract—**In this paper design and simulation of a 10 GHz, divide-by-16…511 programmable frequency divider based on ETSPC and TSPC logic flip-flops in 65 nm CMOS are presented. Main blocks of the divider are three-stage dual modulus divide by 2/3 divider chain, 6-bit counter, jitter removal and synchronisation flip-flops. Extended True Single Phase Clock (ETSPC) logic is used for 2/3 dividers to achieve high input frequency and low power and TSPC logic is used for 6-bit counter. Simulation of the divider was made using Cadence software. Divider's operation frequency is up to 10 GHz. Resulted phase noise is -143.7 dBc/Hz at 1 kHz offset from output frequency and power dissipation is 29.35 mW when input frequency is 10 GHz, division ratio is set to 23, supply voltage 1.2 V. The main application of such divider is as feedback divider in frequency synthesizer for wireless communication systems.**

Index Terms—**CMOS integrated circuits, counter, divider, flip-flop, extended TSPC, high speed, programmable, true-single-phase-clock.**

I. INTRODUCTION

Major challenges for advanced communication circuit designs are high speed, low phase noise and low power consumption. Frequency divider can be one example of such design when it is used as feedback divider in frequency synthesizer for wireless communication systems. In frequency synthesizer output signal of the voltage controlled oscillator (VCO) is input signal for feedback divider. Therefore it operates at highest chip frequencies, what results in increased power consumption, which should be as low as possible for mobile communication devices.

Main block of the frequency divider is a flip-flop. In early CMOS frequency dividers flip-flops based on Razavi topology [1] was used to achieve high frequencies. After some time Wang topology was introduced, which is basically improved Razavi's circuit [2]. Lately flip-flops based on current mode logic (CML) were used for high speed operation. Although able to achieve gigahertz frequencies, all these flip-flops suffer from high power consumption.

CMOS technology scaling allowed usage of low power TSPC flip-flops to achieve required frequencies. TSPC logic and ETSPC (extended TSPC) divider with simplified structure and higher operating frequencies were introduced

in [3] and [4] respectively. In [5] different TSPC and ETSPC structures were extensively analysed.

In this paper we propose novel programmable divide-by-16…511 frequency divider based on ETSPC and TSPC logic flip-flops in 65 nm CMOS technology. Transient and phase noise simulations of designed divider were made using Cadence software. Resulted design and simulation with input frequency up to 10 GHz are presented.

II. DIVIDER'S ARCHITECTURE

Architecture of the divider is shown in Fig. 1. The key blocks are three-stage divide-by-2/3 dual modulus prescaler chain and 6-bit programmable down counter. Signal from input passes three-stage 2/3 prescaler chain after that it is reclocked with jitter cleaning D flip-flop and passed to 6-bit down counter. After counter overflow output signal is generated, reclocked and passed to modin (*MI*) input of the last 2/3 prescaler. Each divider reclocks modin signal and passes it to previous 2/3 cell (up the chain) – frequency of *MI* signal is equal to divider's output frequency, but its duty cycle differs depending on which prescaler reclocks it. If modin signal is high and programming signal *p* is set to high, 2/3 cell divides by 3: cell adds one extra period of cell's input signal to period of cell's output signal. This results in period of three-stage 2/3 prescaler chain output signal equal to [6]

$$T_{out} = 2^3 T_{in} + 2^2 T_{in} p_2 + 2 T_{in} p_1 + T_{in} p_0 =$$
$$= (8 + 4 p_2 + 2 p_1 + p_0) T_{in}, \tag{1}$$

where T_{out} is a period of three-stage 2/3 prescaler's output signal, T_{in} – period of input signal, p_0 - p_2 – binary programming values for 2/3 prescaler 1 to 3 cells, respectively.
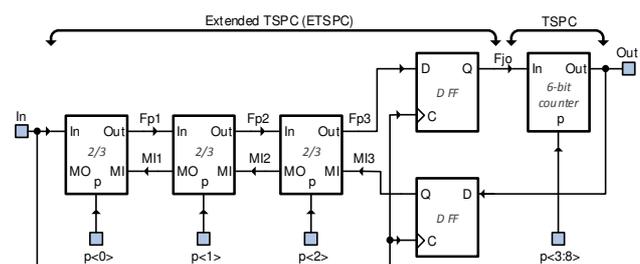
Fig. 1.　Architecture of divide-by-16…511 divider. 2/3 – dual modulus ETSPC prescaler, D FF –D flip-flop.

The output of three-stage 2/3 prescaler chain is asynchronous with respect to the input clock: first prescaler is clocked by VCO output signal, output of the first prescaler clocks second prescaler and output of the second prescaler is input for the third stage. Disadvantage of such asynchronous circuit is accumulation of jitter – jitter of the output signal is sum of jitter in each stage. This can be reduced by using extra flip-flop, clocked by the input frequency, at the end of the asynchronous chain. In such case jitter will be equal to the jitter in the cleaning flip-flop.

Frequency of the 6-bit down counter output signal is much lower than operation frequency of the 2/3 dividers. Also, this signal is delayed by unknown value, depending on division ratio of the counter. To increase synchronization of counter's output signal with three-stage prescaler chain, additional synchronization flip-flop is used in the feedback path between 6-bit counter and third divider. This flip-flop is the same as jitter cleaning flip-flop and also is clocked by input frequency.

A. Dual modulus 2/3 prescaler

The proposed structure of 2/3 prescalers is based on conventional 2/3 divider cell presented in [6]. Two pairs of CML latches are replaced by negative edge triggered ETSPC D flip-flops (Fig. 2, a) similar to [7]. But from [7] our structure differs in logic function integration: to reach higher operating frequencies not only AND gates at inputs of D flip-flops but also NAND gate at the output of D flip-flop in end-of-cycle logic block is combined into D flip-flop (Fig. 2, b). After this upper flip-flop corresponds to prescaler logic block (PL FF) and lower flip-flop corresponds end-of-cycle logic block (EOCL FF) from [6]. Detailed schematics of resulting 2/3 flip-flops are shown in Fig. 3.
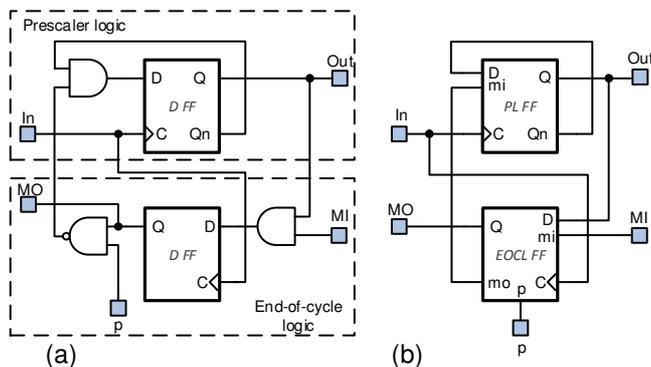
Fig. 2. Structure of 2/3 prescaler. Two pairs of CML latches in conventional 2/3 prescaler are replaced by two ETSPC D flip-flops (a); AND and NAND logic gates integrated into D flip-flops: PL FF – prescaler logic flip-flop, EOCL FF – end-of-cycle logic flip-flop (b).

As we can see from schematics of ETSPC flip-flops, there can be situations, when both transistors of branches, consisting clock transistor, are open during half of the clock period. In this case, output level of the branch is determined by ratio of PMOS and NMOS transistor sizes. Also, this means, that static power dissipation exists in ETSPC flip-flops ant it is higher at lower input frequencies.

Division ratio (2 or 3) depends on *MI* and p signals. *MI* becomes high once in division cycle. It is reclocked and passed to previous 2/3 cell. If programming signal p and *MI* are high, end of cycle logic forces prescaler to swallow one

extra period of input signal. Therefore, instantaneous division ratio is set to 3 only if p and *MI* are high, in other cases division ratio is set to 2.

All stages share same structure showed on Fig. 3. Every stage relaxes operating frequency requirements for next stage: First stage is clocked at maximum input (VCO output) frequency, and maximum input frequency for 2nd and 3rd stages are respectively IN/2 and IN/4 frequency.
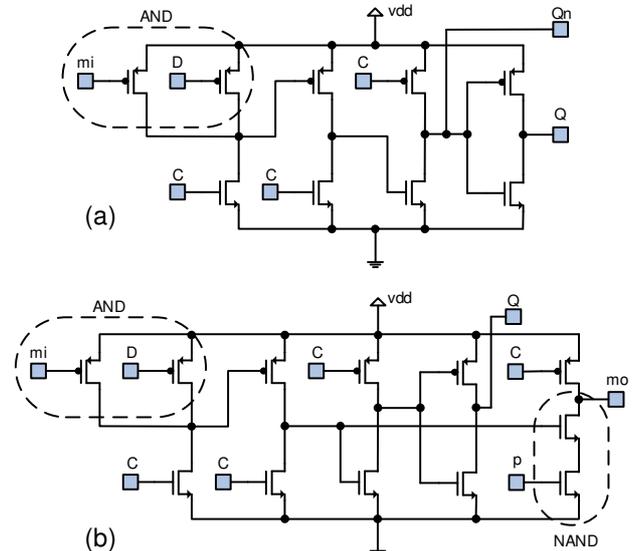
Fig. 3. Schematics of the prescaler logic (a) and end-of-cycle logic (b) flip-flops, based on ETSPC D flip-flop.

As maximum operating frequency is reduced for 2nd and 3rd stages, transistor's sizes are also reduced. This allows to lower power consumption and reduces layout size. Also first 2/3 prescaler does not need modout (*MO*) output, so its circuit is simplified by removing output inverter from end-of-cycle logic flip-flop.

Schematics of jitter cleaning and synchronisation flip-flops are same as of prescaler logic flip-flop, but without AND logic at the input.

B. 6-bit down counter

Structure of 6-bit counter is presented in Fig. 4. it is common structure made of JK/T flip-flops.
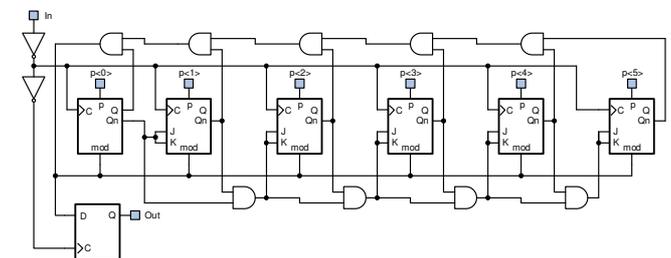
Fig. 4. Structure of 6-bit down counter.

Since counter operates at relatively low frequencies, JK flip-flops are made of TSPC flip-flops. All branches of these flip-flops are always closed between clock signal edges so TSPC logic does not have static power dissipation compared to ETSPC flip-flops.

C. Division ratio control

Division ratio is controlled by 9 bit word. The lowest division ratio is obtained when three dual modulus dividers

are set to divide by 2 mode and counter resets after second bit is set to 1 (divide by 2). In this configuration division ratio is $2^4=16$ and to enable it, control word should be 000010000. The highest division ratio of 511 is obtained when control word is set to 111111111. Values of control word that are lower than 16 (10000) are not used. Control values are summarised in Table I.

TABLE I. DIVISION RATIO CONTROL VALUES.

9-bit Control word, p<8:0>	Division ratio
000000000-000001111	Is not used
000010000	16
000010001	17
…	…
111111110	510
111111111	511

III. SIMULATION RESULTS

Transient and phase noise simulations of designed divider were made using Cadence software. Fig. 5 shows transient simulation results, when supply voltage is 1,2 V, input frequency 10 GHz. Division ratio is set to 23 to check if all 2/3 prescalers operate correctly – this is the hardest operation condition, with highest input frequency and lowest division ratio at which all 2/3 prescalers are set to divide by 3 mode. Names of presented waveforms correspond to signal names, marked in Fig. 1.

Fig. 5. Transient simulation results, when power supply voltage is 1.2 V, input frequency is 10 GHz, division ratio is set to 23, output frequency 434.783 MHz. In – input signal, Out – output signal, Fp1 – Fp3 – output signal of respectively 1 to 3 dual modulus 2/3 prescaler cells, MI1 – MI3 – MI input signal of respectively 1 to 3 dual modulus 2/3 prescaler cells.

Different noise models are analysed in [8]-[10]. Fig. 6 shows phase noise at the output of the divider (Out), before jitter cleaning flip-flop (Fp3) and after jitter cleaning flip-flop (Fjo) at same conditions as transient simulation presented above. Phase noise results is presented as noise level at offset frequency from divider's output frequency (434.783 MHz at this case). As we can see, phase noise at the output is -143.7 dBc/Hz at 1 kHz offset. Also, from this figure we can see, that noise level after jitter cleaning flip - flop is improved by 7.3 dBc/Hz. Achieved noise level allows using this divider in frequency synthesizers for wireless communication systems.
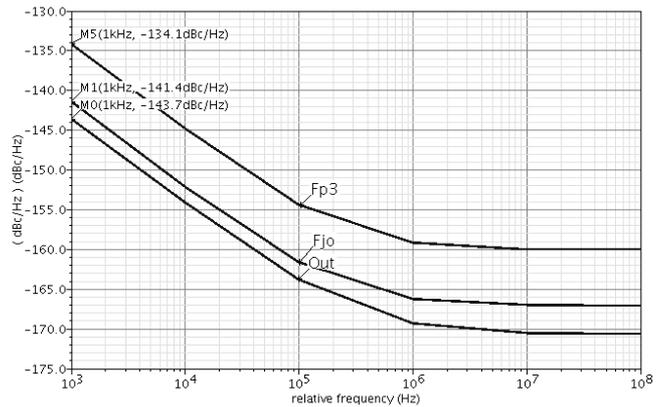
Fig. 6. Phase noise simulation results, when power supply voltage is 1.2 V, input frequency is 10 GHz, division ratio is set to 23, output frequency 434.783 MHz.

To achieve low phase noise, transistors' sizes has to be increased, what results in increased power consumption. Power consumption at these conditions is 29.35 mW.
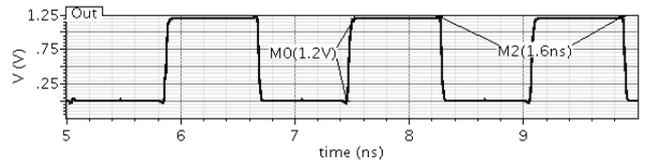
Fig. 7. Output signal, when input frequency 10 GHz, division ratio is set to 16, output frequency 625 MHz.
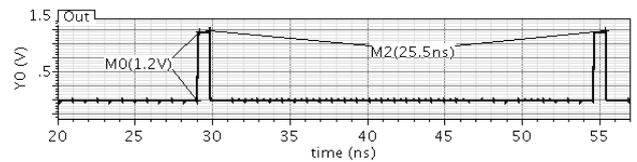
Fig. 8. Output signal, when input frequency 10 GHz, division ratio is set to 255, output frequency 39,216 MHz.
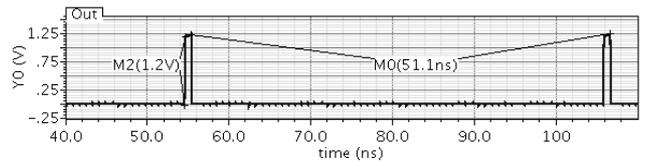
Fig. 9. Output signal, when input frequency 10 GHz, division ratio is set to 511, output frequency 19,569 MHz.

Fig. 7–Fig. 9 show transient simulation results when division ratio is set respectively to 16 (lowest division ratio), 255 and 511 (highest division ratio).

IV. LAYOUT

Layout of the designed divider is presented in Fig. 10. It occupies 620 µm × 120 µm area of silicon. Biggest area is taken by 6-bit counter, since it is made of TSPC flip-flops, consisting of more elements compared to ETSPC flip-flops.

6-bit counter

2/3 prescaler chain, jitter cleaning and synchronisation flip-flops
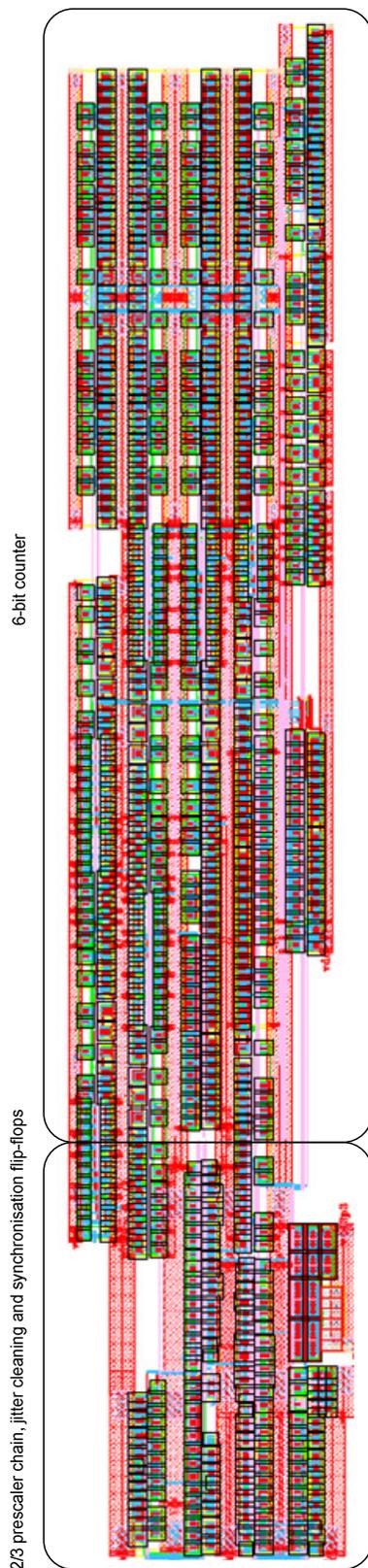
Fig. 10. Layout of programmable divide-by-16...511 divider.

V. CONCLUSIONS

Novel programmable divide-by-16…511 frequency divider based on ETSPC and TSPC logic flip-flops is designed in 65 nm CMOS technology. Main blocks of the divider are three-stage dual modulus divide by 2/3 prescaler chain, 6-bit counter, jitter removal and synchronisation flip-flops. Simulations show that divider's operation frequency is up to 10 GHz. The hardest operation condition is at highest input frequency and division ratio of 23 at which all 2/3 prescalers are set to divide by 3 mode. So, resulted worst phase noise is -143.7 dBc/Hz at 1 kHz offset and power dissipation is 29.35 mW when input frequency is 10 GHz and division ratio is set to 23, power supply voltage 1.2 V. Achieved parameters allow to use this divider in frequency synthesizers for wireless communication systems.

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