Development of a Wireless Low Power Datalogger with High Performance Converter

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***Abstract*—In this work, a low power datalogger with a wireless connection is described. The datalogger can be used as a portable and stand-alone device, as well as a wireless sensor network node. A flexible architecture, which combines a microcontroller with external local buses (data and address) and a complex programmable logic device (CPLD), has been used. The system has two special characteristics: one of them is the high resolution of A/D converters; the second is based on the incorporation of a non-volatile random-access memory (NVRAM) that allows fast access to stored data and a low consumption. Storing data in an NVRAM implies an extra security level for the maintenance of data even when the batteries of the system have been exhausted. The complete glue logic has been integrated into a Zero-Power CPLD in order to reduce size. In addition, in each specific application, the CPLD allows the implementation through hardware of some interfaces to sensor module, saving computation time.**

***Index Terms*—CPLD, data acquisition, energy-saving systems, microcontroller, sensor networks.**

I. INTRODUCTION

In many applications, data acquisition must be developed in places where an electrical connection is not available or where its access is difficult to reach. In these situations, a sensor network or a portable datalogger can be used. In both cases, the use of an energy-saving system, which can be supplied by harvesting energy, is essential.

Nowadays, one of the main objectives of portable devices and sensor networks is based on getting a long duration of the battery. In this sense, several studies focused on increasing the battery capacity, decreasing the circuit consumption, and using self-generating energies [1], [2] (such as solar and wind energy [3]) have been proposed. The efficiency of current systems allows a total (or partial) recharge of the batteries of low consumption systems.

Figure 1 and Fig. 2 show the classic hardware structure of a sensor network node [4] and the structure of a simple portable module, respectively. In both cases, the mass storage module is not used, although this module could have been included.

The similarity of the hardware structure between both applications can be observed. It is possible to have a single system that covers both situations. Although the datalogger is not part of the sensor network, the wireless communication allows for an easy data download.

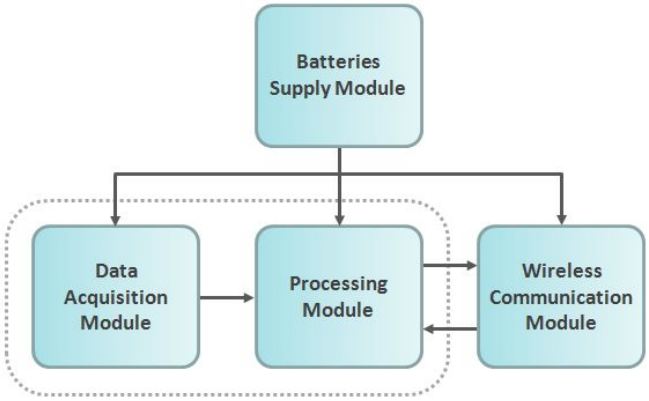

Fig. 1. HW structure of a wireless node.

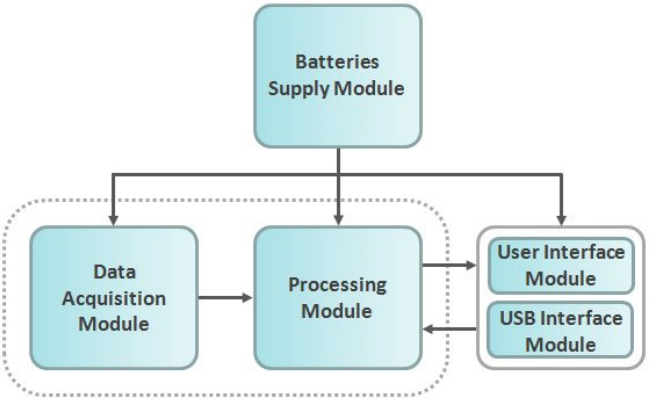

Fig. 2. HW structure of a portable acquisition module.

In the case of using the system as a portable module, a higher number of peripherals are required to perform the user interface. On the other hand, any mobile or wireless

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communication module can be connected. The radio frequency (RF) module does not have to be integrated in the same printed circuit board (PCB).

The huge success of wireless data transmission networks caused the development of many low consumption nodes. Among these nodes, the motes from the companies Crossbow [5] or Moteiv [6] are included, where characteristics such as a small size or a low consumption are essential in their design. However, these devices have a lower performance in the data acquisition module, and they include low-cost sensors which are not useful for applications where a sensor with a high precision is required. In addition, in many cases, these motes do not have an external instrument interface. In order to solve these problems, in many works, a design of customized motes for different applications, has been used. In [7] the design of a mote with interfaces for precision horticulture is presented. Other works describe the design of nodes for irrigation control systems, as [8] (with a node powered with solar energy) and [9] (that presents a node with adaptive control).

Another limitation presented in these motes is related to the possibilities of peripheral connections. These possibilities are associated to the specific interfaces of the microcontroller included in the mote, or the feasibility that these connections can be emulated by the I/O ports of the microcontroller. For example, in the motes commented previously, a parallel NAND flash memory would be difficult to connect, although several works (such as [10]) indicate that this memory is the most energy efficient storage device for sensor networks. In the same way, the memory size for code and/or data is limited by the internal microcontroller memory. A similar analysis can be developed for low cost dataloggers based on a specific microcontroller.

The aim of the design of this first datalogger prototype has been the development of a system with high resolution converters and other additional performances in the data acquisition module. On the other hand, another essential feature of this design is based on the development of a flexible architecture that allows the system evolution without being limited to a specific microcontroller, and maintaining a low consumption. This is achieved using a microcontroller, with data and address buses external to the chip, so that it easily allows the addition of coprocessors and peripherals mapped in the microcontroller memory in future prototypes. This allows a fast access saving computing time, and providing possibilities of increasing the memory capacity (with a size as large as required by the application), using hardware paging.

The structure of this paper is as follows. The datalogger, named UCOADP, is presented and described in Sections II, and III. On the other hand, an analysis of the consumption is illustrated in Section IV, where a comparison with other nodes is included. Finally, Section V summarizes the main conclusions of this work.

II. Requirements of the Acquisition Module

The main goal of the design of the datalogger is to achieve a data acquisition module with high performances and a low power consumption, so that the module can have a power supply with batteries or a self-generating energy system. In this way, a high autonomy is obtained.

In addition to the high autonomy requirement, it is also important to have an SRAM of the largest possible capacity in order to create data buffers. Data buffers are essential in embedded applications, where the processing of the information must continue while the data transfers are completed. Although a SRAM could have been used, an NVRAM with real-time clock (RTC) has been selected with the objective that the acquired data or configuration parameters are not lost when the batteries are exhausted. The digital part of the system has a different power supply to the analog part, in order to reduce the power consumption. A power supply voltage of 3.3 V is applied to the digital part, while the analog part can operate on a voltage of 3.3 V to 5 V. With a power supply of 5 V, the A/D converter input range is increased.

The main features of the UCOADP datalogger, based on the MSC1210 microcontroller from Texas Instruments [11], are the following:

– A/D converter with a programmable resolution from 8 to 24bits.

– 7 single or differential, unipolar or bipolar input/analog channels.

– A 128KB NVRAM with a RTC to store the acquired data. This allows not to lose the data in the case of a power failure.

– Clock alarm with programmable interrupts which allows setting the year, month, day, and hour with a resolution of a second. This feature facilitates the acquisition of the samples at very low frequencies.

– User interface: LCD and keyboard matrix circuit.

– USB interface for data communication or in-system programming of the microcontroller.

Figure 3 illustrates the entire system ready to work as a portable module. In the case of using the system as a part of a wireless data transmission node, a wireless communication module must be connected. In addition, the peripherals that interact with the user (as the buzzer or LCD and keyboard interfaces) should not be assembled; this allows a decrease of the power consumption.

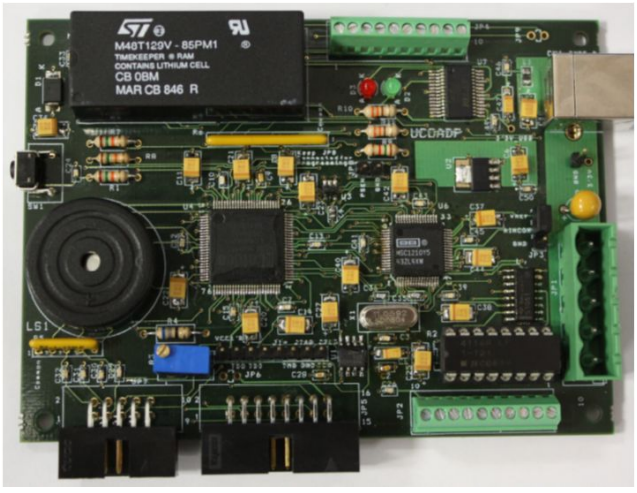

Fig. 3. UCOADP datalogger.

III. Hardware Description of the DATalogger

The block diagram of the UCOADP module is illustrated in Fig. 4. The following blocks are included: connector

block, control block, memory block with RTC, A/D converter block, digital I/O block, peripherals block, and power supply block. A brief description of these blocks is shown below.

A. Connectors Block

The target has mechanically robust elements to connect the analog signals that are acquired. The supply voltage of the A/D converter and its reference voltage are also available in this connector. Thus, another board can be connected to manipulate the analog signals and take advantage of the input range and the resolution of the converter.

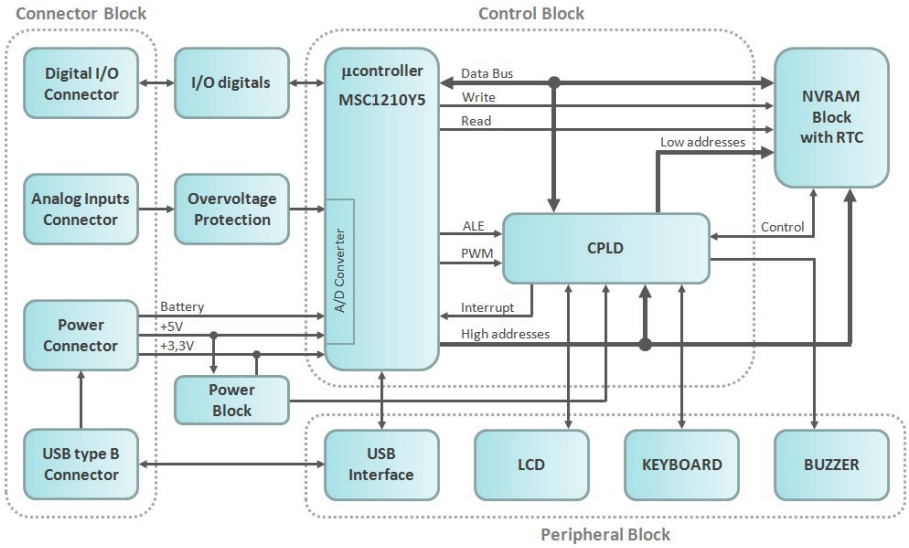

Fig. 4. Block diagram of the UCOADP module.

B. Memory Block and RTC

The on-chip SRAM and the non-volatile storage capacity of low power microcontrollers is quite small. Because of this, an NVRAM, contained in an M48T129V integrated circuit from ST Microelectronics [12], has been included in the system. In addition to a 128KB memory capacity, this circuit has a real-time clock and a lithium battery. The use of an NVRAM with lithium battery allows the replacement of the batteries without losing the data and the configuration parameters programmed by the user. On the other hand, the NVRAM can also be used as main memory in our system for the remote update of the application, allowing the execution of the firmware update of the microcontroller internal memory.

Other advantage of using an NVRAM instead of another type of memory (such as a flash memory) is based on the fact that the NVRAM is a read-write memory and, therefore, the access to the stored data is simple and fast. Flash memory needs a programming algorithm and, for this reason, the time to store data is greater than in the case of an NVRAM. The consumption of different types of flash memories in sensor network nodes is included in [10].

On the other hand, the M48T129V circuit has a small current consumption (about 3 mA in standby-mode and 50 mA in access-mode). This last value is high, but the advantage of this circuit versus a flash memory is that its access is faster, so that, the energy consumption is lower. Even so, if the standby consumption is not permissible, the system has a MOSFET which controls the NVRAM supply. If the application does not use the RTC to return the microcontroller to active mode, the NVRAM can be disconnected from the system supply.

For the application proposed with this module, the sampling period is low and the accesses are fast, therefore, the average consumption of this module can be considered as the consumption in the standby-mode.

The RTC provides time and date in the format of year, month, day, hour, minute and second, and allows the programming of an alarm with a resolution of a second, which activates an interrupt request. In the absence of power supply, the M48T129V has 10 years of data retention for the NVRAM and the date provided by the RTC. In case of being required an NVRAM with a higher capacity, it can be installed with minimal modifications in the system.

C. Control Block

This block is composed by an MSC1210 microcontroller from Texas Instruments and an LC4064ZC CPLD from Lattice Semiconductor [13] (if a CPLD with a greater performance is desired, other pin-compatible CPLDs from the same family, with a higher number of macrocells, can be used). The main function of this block is the control of the acquisition and storage of samples in the memory block and, on the other hand, the control of peripheral devices.

The incorporation of a CPLD to the system greatly increases the flexibility to connect peripherals (integrating the complete glue logic) [14]. Also, it allows its reconfiguration (according to each application) to implement some interface and specific communication protocols to sensor module. This quality distinguishes the system from the others. The interface of this type of sensors is achieved by hardware realization, while in many other motes, a software realization is required. In this case, the time employed in the communication is reduced and there is no processing time consumption.

An alternative to the CPLD is the use of a field-programmable gate array (FPGA) for the node of sensors [15]. Other authors use a commercial board to build a stand-alone platform [16]. This commercial board combines a Spartan-3 (XC3S2000), a CPLD and a 128Mb flash

memory. The CPLD performs the interface between the FPGA and the flash memory. In [17], the authors propose the implementation of a mote from Crossbow in a CoolRunner-II CPLD form Xilinx. The CPLD performs the XMesh's Cost Functions and Header CheckSum of the XMesh Routing Layer from Crossbow. This implementation accelerates the Cost Estimation algorithm of the XMesh routing protocol by 606 times and, at the same time, there is a reduction in the measured energy consumption by 97 %. However, these improvements have not been compared with the power consumption of the CPLD in the overall system, when the CPLD is not performing these algorithms.

Using an FPGA increases the possibilities of the node, but it also increases the cost and power consumption as compared to the CPLD. For this reason, the CPLD has been chosen instead of the FPGA for the datalogger development.

The MSC1210 architecture is fully compatible with the standard 8051 instruction set, but it includes some improvements which reduce the implementation cost of the datalogger. Among these improvements, it should be highlighted an additional 32-bit accumulator and a faster execution. Specifically, the execution of the MSC1210 is up to three times faster than the standard 8051 core (given the same external clock source), and it achieves the same performance at lower power than the standard 8051 core. On the other hand, it has a great performance in terms of consumption, characteristics of conversion process, and availability of peripherals.

The LC4064ZC CPLD has 64 macrocells that allow the implementation of the whole control logic of the block on a chip:

– Reset signal generation of the microcontroller.

– Control of the access to the LCD through hardware for a programming simplification.

– Address decoder to generate chip select signals of the memory and peripherals.

– Generation of A16 address line to the memory.

– Control of a permission bit to enable the change of value in the A16 bit.

– Keyboard control: row generation and reading of column status.

– Interrupt controller with two interrupt requests: RTC alarm and keyboard.

This CPLD has been selected because its current consumption in static mode is about 10 µA, especially in those applications where the microcontroller turns to low consumption modes. As the core dynamic power is about 1.8 V, the consumption is much reduced (in the order from 100 µA at 1 MHz). A technique used in order to reduce the CPLD consumption is based on controlling its clock signal by the microcontroller. The CPLD only uses the clock signal when specific peripherals (such as the LCD and the buzzer) are being used. If these peripherals are not used, the microcontroller does not generate the clock signal and, therefore, the CPLD consumption is lower.

Usually, the acquisition frequency, in applications where the datalogger is used, is low (up to 1 Kmps, and even less than 1 mps). In this last case, MSC1210 can be configured in idle mode to reduce consumption. In order to put it into active mode, the interrupt produced by one of the internal timers, or by the CPLD, can be used when an acquisition is performed. Also, if a key is pressed, the CPLD can initiate an interrupt request to the microcontroller; so that the user can activate the idle-mode if the module is inactive for a certain period of time. In order to return the microcontroller to the active-mode, the user has two options: firstly, the user can decide if the RTC will activate an interruption to return the microcontroller from idle to active-mode; secondly, the user can decide to return to active from stop-mode via a power-on reset.

D. A/D Converter Block

The MSC1210 integrates an A/D converter with 24 bits of resolution and 8 inputs channels, which can be configured as differential/single-ended and unipolar/bipolar channels. On the other hand, it also has a programmable gain amplifier (from 1 to 128) and a generator of precision voltage reference. These features allow the implementation of a datalogger with an excellent performance and a low cost.

As it was described in Section III.A, the converter has 7 analog input channels, because one of them is used to monitor the battery status. A protection circuit, composed by an array of Schottky diodes and resistances in series, is included to protect the converter from an overvoltage that exceeds the allowed voltage range.

E. Digital I/O Block

This block consists of a 6-bit digital port, a 16-bit PWM, and two 16-bit timers. The block is implemented by the peripherals integrated in the MSC1210.

The digital port lines are bi-directional and each of them can be programmed independently as input or output/input. These lines can also be used as I/O ports if the PWM output and the timers inputs are not used.

F. Peripherals Block

The USB interface, an LCD, a keyboard and a piezoelectric buzzer are included in this block.

The USB interface has been developed by the FT232RL circuit from FTDI [18]. This circuit has a power supply of 5 V provided by the USB connector and it is only used when a PC is connected for the programming of the microcontroller firmware or the transfer of the samples acquired and stored in the NVRAM.

The LCD is an alphanumeric dot matrix type backlight device with 2 rows and 16 columns. A MOSFET driver has been included to control the LCD supply voltage and the backlight, reducing the power consumption. The driver is controlled through software with a register implemented in the CPLD.

The keyboard is of matrix type with a structure of 4 rows and 4 columns and it is controlled by software with the CPLD. This programmable device activates the rows by a program and implements a read port to check the column status and determine if a key has been pressed.

The piezoelectric buzzer is controlled by the CPLD via the PWM output of the MSC1210 which determines the acoustic signal frequency. The operation of this buzzer is enabled by a register implemented in the CPLD.

G. Power Block

This module can be supplied by rechargeable batteries, the USB connector, or a self-generating energy module. The

target includes a dropout voltage regulator that, from a 5 V input onward, generates a voltage of 3.3 V for the microcontroller, the NVRAM and the CPLD. As this CPLD needs a voltage of 1.8 V, a regulator (that generates 1.8 V from the voltage of 3.3 V) has been included.

IV. POWER CONSUMPTION

A very important feature of the developed system has been the power consumption reduction when the circuit is acquiring samples, or when it is in idle-mode.

The system has been developed to operate at 3,3 V, which is a current trend in the framework of external sensor interconnections, against the traditional use of 5 V. For example, in the case of the MSC1210 microcontroller working at 8 MHz, the typical consumption goes from 15 mA (powered with 5 V) to 8 mA (powered with 3.3 V). This supply voltage restricts the input voltage range of the converter. Even so, as a voltage higher than 3.3 V can be supplied, the input voltage for the acquisition section of the microcontroller can be up to 5 V. On the other hand, as the system acquires samples at low frequency, a microcontroller, characterized by a low consumption in idle-mode and high performance in the acquisition module, has been selected. The MSC1210 microcontroller has another mode (stop-mode) with a lower consumption than the idle-mode, but this cannot be used in all applications. For this reason, the idle-mode has been used in this design.

The number of circuits is low; even so, each component has been analysed in order to decide its integration in the system with the goal of decreasing the consumption. A study of these circuits in terms of performance and consumption is detailed below.

The system is based on a microcontroller with internal flash memory; so, a complete datalogger could be integrated in an only circuit. However, as one of the goals is the development of a system that can acquire samples in an autonomous way at a desired frequency, the microcontroller will stay in idle-mode until an external clock activates the microcontroller to perform an acquisition. For this task, an external calendar clock must be included. In the case of a sensor network, this task can be carried out by the RF module, but an always-on active RF module would be necessary, and this would increase the consumption. For example, the CC2420 RF module from Texas Instruments [19] has an RX consumption of 19 mA, and XBee module from Digi International [20] has an RX consumption of 50 mA.

Due to the fact that the use of an external calendar clock is required, several NVRAMs, available in the market, with a calendar clock integrated and a low consumption, can be selected. As it has been described in previous sections, the use of an NVRAM allows that the acquired samples are not lost after a power supply failure. Also, the storage of the acquired data is faster than other systems (such as flash memories), reducing consumption.

A decoder circuit is required due to the use of an external calendar clock. For this task, the CPLD can be used. The LC4064ZC CPLD has been selected because it is classified as a Zero-Power CPLD. This device only has a current consumption of 11µA when there is not activity in its input and output ports. Then, the consumption of this CPLD is very low when the microcontroller is in idle-mode. In addition, the CPLD inclusion allows increasing the number of digital inputs and outputs, as well as the inclusion of other peripherals (such as a LCD or a piezoelectric buzzer).

In Table I, the consumption of the UCOADP module is shown, according to the typical consumption of each component (specified in the datasheets from the manufacturers). Table II includes the experimental data for an 8 MHz frequency.

TABLE I. TYPICAL COMSUPTION ACCORDING TO THE MANUFACTURERS.

Component	Active mode	Idle mode
Microcontroller at 3.3 V	9 mA	<1 mA
Analog part of the microcontroller at 3.3 V	1 mA	1 mA
NVRAM	50 mA	3 mA
CPLD	80 µA	11 µA

TABLE II. EXPERIMENTAL RESULTS OF CONSUMPTION AT 8 MHz.

Component	Active mode
Microcontroller at 3.3 V (analog part included)	8.96 mA
Microcontroller + CPLD	10.54 mA
Microcontroller + CPLD + NVRAM	11.67 mA

Figure 5 illustrates the consumption of UCOADP target versus frequency, obtained experimentally with all the components integrated. The measures have been made in the lab using high quality instruments, which allow measure the current consumption, and easily modify the frequency. To measure the current consumption, an ammeter has been used. In order to generate the clock frequency, a precision signal generator and an oscilloscope have been used, with the objective of having two independent measures. To develop the measures, a microcontroller has been integrated into a PCB, and later, the components have been soldered. About the working mode of the microcontroller and the software executed, the measures have always been made in active-mode, with a test application which activates all the microcontroller peripherals and access to all the external peripherals. This application has a user interface via the microcontroller serial port, and it has been used to check all the components once the board is developed.

As it can be seen in Fig. 5, consumption increases with frequency. This increase is more remarkable for frequencies from 2 MHz to 12 MHz. However, this increase is not significant for frequencies lower than 2 MHz. Specifically, for a frequency of 1 MHz, the consumption is 2 mA and, for 100 KHz, the consumption is 1 mA. Hence, the ideal frequency value of the microcontroller is 1 MHz in order to achieve a good performance with a minimal power consumption.

Table III shows the consumption related to the acquisition of other modules, without taking into account the wireless communication consumption. This table is merely illustrative; a more detailed study must take into account the sensors connected to the device and the application scenario, such as [21]–[26].

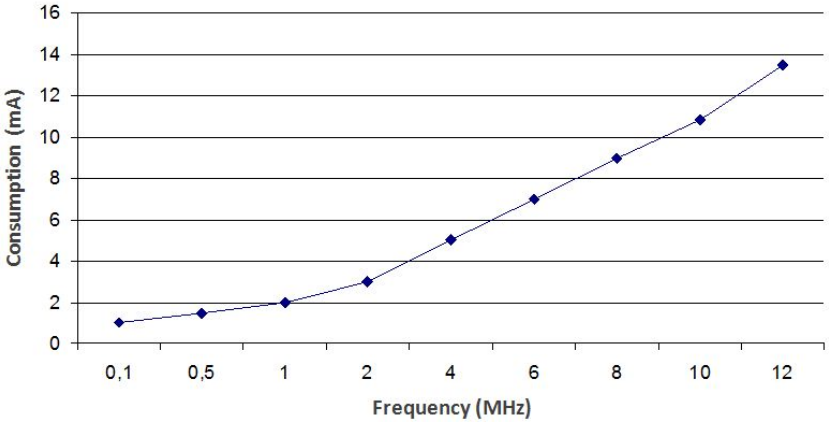

Fig. 5. Consumption versus frequency of the UCOADP module.

Mica2 module has a similar consumption to UCOADP. The other modules have a lower consumption, because of the use of the ultra-low power MSP430 microcontroller from Texas Instruments; however, this microcontroller is a monolithic system and, hence, it presents a lower flexibility. In addition, these modules have a lower non-volatile memory capacity than UCOADP. On the other hand, as UCOADP uses a CISC processor and a CPLD, it can achieve the same processing capacity using a lower frequency of 1 MHz with a similar consumption (2 mA as it can be seen in Fig. 5) to Telos and Tmote Sky. These two commercial motes cannot achieve the same processing capacity using a lower frequency because they use a RISC processor.

Finally, in Table IV, a comparison of characteristics between different data acquisition modules is illustrated. As it can be seen in this table, UCOADP module has the converter with the highest resolution and it is the only one which includes a PGA. Although the resolution of the converters embedded in the microcontroller can be increased using additional external electronics [27], this would increase the complexity of the system and the consumption.

TABLE III. CONSUMPTION OF OTHER MODULES AT 8 MHz.

Module	Active mode
Mica2 (Crossbow)	8 mA
Telos (UC Berkeley)	1.8 mA
Tmote Sky (Moteiv)	2.4 mA

TABLE IV. COMPARISON OF DATA ACQUISITION CHARACTERISTICS.

Module	Converter	PGA
UCOADP	24 bits	Yes
Mica2 (Crossbow)	10 bits	No
Telos (UC Berkeley)	12 bits	No
Tmote Sky (Moteiv)	12 bits	No

V. CONCLUSIONS

The portable UCOADP datalogger has been described in this paper. A new architecture, based on the combination of a microcontroller with access to an external memory and a CPLD, has been presented. This architecture is more flexible than the most popular motes, because it easily allows to increase the memory and to connect new peripherals. Besides this architecture also allows the remote update of the application because the external memory can be easily mapped and configured as data and program memory accessing to the implemented registers in the CPLD for that purpose.

The highlight of this design is the use of an NVRAM memory with RTC that allows saving power consumption in case of making acquisitions at very low frequencies (because the system can stay in idle-mode between acquisitions). In addition, in the case that the system is embedded in a wireless sensor network, it allows activating the RF module to transfer data blocks instead of punctual data. On the other hand, if the battery is exhausted, the acquired data and the configuration parameters are not lost and can be extracted when the module is power supplied again.

The use of a NVRAM not only allows to put the microcontroller into idle-mode faster; besides, it also can be used as a data buffer and not only as data storage in the applications.

Another original feature of this system is based on the combination of a microcontroller with a low-power CPLD. This reconfigurable device allows reconfiguring the system to provide it with a hardware interface for intelligent sensors or other specific interfaces. On the other hand, the complete glue logic has been integrated into the CPLD.

Finally, as it is shown in the paper, the microcontroller used in the datalogger has high resolution converters and programmable-field amplifier, presenting a similar consumption to other commercial modules.

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